UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,651	12/31/2001	Howard S. David	42390.P13872	9227

8791 7590 03/30/2004

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	6

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/039,651	Applicant(s) DAVID, HOWARD S.
	Examiner Zhuo H. Li	Art Unit 2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 12/31/2003 (paper no. 5).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 25-28 are rejected under 35 U.S.C. 102(e) as being anticiapted by Stracovsky et al. (US PAT. 6,216,178 hereinafter Stracovsky).

Regarding claim 25, Stracovsky discloses a method comprising delivering during a first plurality of transfer periods information corresponding to both an activate command and a cache fetch command from a memory controller (104, figure 1) to a memory module (108, figure 1) over a memory bus, and from the memory controller to the memory module delivering during a last transfer period information differentiating between an activate command and a cache fetch command (figures 1A-3B and col. 5 line 49 through col. 9 line 15).

Regarding claim 26, Stracovsky discloses the method wherein delivering during a last transfer period information differentiating between an activate command and a cache fetch command includes delivering cache hit information (col. 6 line 50 through col. 7 line 55).

Regarding claim 27, the limitations of the claim are rejected as the same reasons set forth in claim 25.

Regarding claim 28, the limitations of the claim are rejected as the same reasons set forth in claim 26.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,178 hereinafter Stracovsky) in view of Yoo et al. (US 2002/0129215 hereinafter Yoo).

Regarding claim 1, Stracovsky discloses a universal controller (104, figure1A) operated as a memory controller comprising an array of tag address locations (114, figure 1B) and a command sequence and serializer unit (116, figure 1B) to control a memory module (108, figure 1A), the command sequencer and serializer unit to control the memory module by delivering a plurality of commands (220, figure 1B) over a plurality of command and address lines, the

command delivered over a plurality of transfer periods, the plurality commands including an active command and a cache fetch command, the active command and cache fetch commands different in format only in the information delivered during a last transfer periods (figures 1A-3B and col. 5 line 49 through col. 9 line 15). Stracovsky differs from the claimed invention in not specifically teaching a data cache located on the memory module so that the command sequencer and serializer unit controls the data cache located on the memory module. However, Yoo discloses a data buffer (48, figure 1) operated as a data cache located on a memory module (42A) so that a memory controller (40, figure 1) controls the data buffer located on the memory module in order to increase data transmission rates in a memory system (abstract and [0028] through [0038]). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Stracovsky in having the data cache located on the memory module so that the command sequencer and serializer unit controls the data cache located on the memory module, as per teaching of Yoo, in order to increase data transmission rates in a memory system.

Regarding claims 2-6, Stracovsky teaches the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period and each of the activate and cache fetch command including memory module destination information during a first transfer period and row address information during each of the four transfer periods, wherein the cache fetch command includes way information delivered during the last transfer period and the plurality of commands each delivered over four transfer periods (col. 6 line 50 through col. 7 line 55).

Regarding claims 7-12, Stracovsky teaches the plurality of commands further including a read command and a read and preload command differing in format only in the information delivered during a last transfer period and differing in cache hit information delivered during the last transfer period, wherein the read command and the read and preload command includes memory module destination during a first transfer period and column address information during each of the four transfer periods, and wherein the read and preload command includes way information delivered during the last transfer period and the plurality of commands each delivered over four transfer periods (col. 6 line 50 through col. 7 line 55).

Regarding claim 13, Stracovsky discloses a memory module (108, figure 1A) controlled by a plurality of commands delivered by a universal controller (104, figure 1A) operated as a memory controller over a memory bus, the memory controller includes an array of tag address storage locations (114, figure 1B), the commands delivered over a plurality of transfer periods, the plurality commands including an active command and a cache fetch command the active command and cache fetch commands different in format only in the information delivered during a last transfer periods (figures 1A-3B and col. 5 line 49 through col. 9 line 15). Stracovsky differs from the claimed invention in not specifically teaching the memory module comprising at least one memory device and a data cache coupled to the memory device so that the data cache is controlled by the plurality of commands delivered by the memory controller. However, Yoo discloses a memory module (42A, figure 1) comprising at least one memory device (44, figure 1) and data buffer (48, figure 1) operated as a data cache coupled to the memory device so that the data buffer is controller by a plurality commands delivered by a memory controller (40, figure 1) over a memory bus (56, figure 1) in order to increase data transmission rates in a memory system

(abstract and [0028] through [0038]). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Stracovsky in having the memory module comprising at least one memory device and a data cache coupled to the memory device so that the data cache is controlled by the plurality of commands delivered by the memory controller, as per teaching of Yoo, in order to increase data transmission rates in a memory system.

Regarding claims 13-18, the limitations of the claims are rejected as the same reasons set forth in claims 2-6.

Regarding claim 19, Stracovsky discloses a system comprising a processor (102, figure 1A), a universal controller (104, figure1A) operated as a memory controller comprising an array of tag address locations (114, figure 1B) and a command sequence and serializer unit (116, figure 1B) coupled to the array of tag address storage location, and a memory module (108, figure 1A) coupled to the universal controller via a memory bus, the memory module controlled by a plurality of command delivered by the universal controller, the commands delivered over a plurality of transfer periods, the plurality commands including an active command and a cache fetch command the active command and cache fetch commands different in format only in the information delivered during a last transfer periods (figures 1A-3B and col. 5 line 49 through col. 9 line 15). Stracovsky differs from the claimed invention in not specifically teaching the memory module comprising at least one memory device and a data cache coupled to the memory device so that the data cache is controlled by the plurality of commands delivered by the memory controller. However, Yoo discloses a memory module (42A, figure 1) comprising at least one memory device (44, figure 1) and data buffer (48, figure 1) operated as a data cache coupled to

the memory device so that the data buffer is controller by a plurality commands delivered by a memory controller (40, figure 1) over a memory bus (56, figure 1) in order to increase data transmission rates in a memory system (abstract and [0028] through [0038]). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Stracovsky in having the memory module comprising at least one memory device and a data cache coupled to the memory device so that the data cache is controlled by the plurality of commands delivered by the memory controller, as per teaching of Yoo, in order to increase data transmission rates in a memory system.

Regarding claims 20-24, the limitations of the claims are rejected as the same reasons set forth in claims 2-6.

Response to Arguments

6. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jhang (US PAT. 6,253,292) discloses a distributed shared memory multiprocessor system based on a unidirectional ring bus using a snooping scheme (abstract).

Santeler et al. (US PAT. 6,430,702) discloses a computer system having a memory controller to access a plurality of memory module in response to an interaction with a central processing unit (figure 3 and abstract).

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any response to this final action should be mailed to:

BOX AF

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 308-6606

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li

Art Unit 2186

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100